UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/826,744	04/16/2004	John Harper	P3356US1 (119-0036US)	1362

61947   7590   11/24/2009
WONG, CABELLO, LUTSCH, RUTHERFORD & BRUCCULERI LLP
20333 SH 249
SUITE 600
HOUSTON, TX 77070

EXAMINER
MCDOWELL, JR, MAURICE L

ART UNIT	PAPER NUMBER
2628	

MAIL DATE	DELIVERY MODE
11/24/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

<table>
<tr><td rowspan="2"><i>Office Action Summary</i></td><td colspan="2">Application No.</td><td colspan="2">Applicant(s)</td></tr>
<tr><td colspan="2">10/826,744</td><td colspan="2">HARPER, JOHN</td></tr>
</table>

	Application No.	**Applicant(s)**
Office Action Summary	10/826,744	HARPER, JOHN
	Examiner	**Art Unit**
	MAURICE MCDOWELL, JR	2628

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>10 August 2009</u>.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) <u>76-80</u> is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) <u>76-80</u> is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☐ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO/SB/08)
    Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date _____.

5)☐ Notice of Informal Patent Application

6)☐ Other: _____.

DETAILED ACTION

Response to Arguments

1.   Applicant's arguments filed 8/10/2009 have been fully considered but they are not

persuasive.

2.   Applicant argues: The Examiner asserts that "generation of frames is equivalent to

applying a first effect." Office Action dated 12 May 2009 at p. 2. However, this is clearly

incorrect because the plain language of the claim states "to apply a first effect to a first frame of

said image." Because the effect is being applied to a frame, the frame must have already been

generated. In the context of Giles the "generation of frames" has to do with a timing function of

the emulator relative to the target computer system. As stated above, Giles monitors the time

taken by the emulator to generate frames to determine if the emulator must skip frames in order

to stay in sync. Therefore, the generation of frames disclosed in Giles is in no way equivalent to

applying effects to frames.

3.   Examiner respectfully disagrees: Giles does teach generation of frames is equivalent to

applying effects to frames, (see col. 2 lines 53-60) (Upon detecting a frame end, the emulation

module executes...so as to at least partially render a frame...evaluates the ability of the general

purpose computer to generate video frames fully synchronized with the target computer system.)

4.   Applicant argues: As stated above, Glanville is simply directed to splitting up the

graphics code between an ASIC and a CPU. The code is not split with any recognition of frames.

Rather the code is split via software analysis such that the CPU performs the operations that

cannot be performed by the ASIC. Glanville is completely silent as to at least both of these

elements. Glanville does not disclose any kind of temporal division of work between two

processors because Glanville only discloses splitting code based on capabilities of processors not

timing. Furthermore, Glanville is completely and utterly silent as to applying effects to frames by

one processor and then another processor.

5.   Examiner respectfully disagrees: The code in Glanville is split with recognition of

frames, (see [0321]) (If the current vertex program is nonexistent or the "point" is culled, the

current raster position and its associated data become...); Thus Glanville teaches splitting code

with recognition of frames because the current raster position is tracked. Glanville does disclose

temporal division of work between two processors, (see [0070]) (A program can be split into two

(2) parts with the CPU 106 emulating some of the computations, and the ASIC 102 executing the

remainder); Further see [0061], (A particular hardware implementation (i.e., ASIC 102) may

have timing latencies where the result of an instruction will not immediately be available for use

as input to a subsequent instruction); Thus Glanville teaches because Glanville is concerned with

timing latencies and dividing work.

Claim Rejections - 35 USC § 103

6.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in
>
> section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are
>
> such that the subject matter as a whole would have been obvious at the time the invention was made to a person
>
> having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the
>
> manner in which the invention was made.

7.   Claims 76-80 are rejected under 35 U.S.C. 103(a) as being unpatentable over Giles Patent

No.: 6,115,054 in view of Glanville et al. Pub. No.: US 2003/0009748 A1.

8.   Regarding claim 76, Giles teaches: A method of applying two effects to an image, the
method comprising the steps of - using a first microprocessor to apply a first effect to a first
frame of said image, said first microprocessor applying said first effect while emulating a second
microprocessor (fig. 11A, 384 see also col. 16 lines 23-35) (The generation of frames is
equivalent to applying a first effect).

9.   Giles doesn't teach: -using said second microprocessor to apply a second effect to said
first-effected frame, applying said first effect to a next frame by said first microprocessor
approximately during the time that said second microprocessor is applying said second effect to
said first-effected frame.

10.   The analogous prior art Glanville teaches: -using said second microprocessor to apply a
second effect to said first-effected frame, applying said first effect to a next frame by said first
microprocessor approximately during the time that said second microprocessor is applying said
second effect to said first-effected frame (fig. 6, 606 see also [0084]) (The portion of graphics
processing performed on ASIC is equivalent to 2nd processor applying effect to first frame) for
the benefit of providing a set of API features that facilitate combining application-programmable
vertex processing with existing 3D applications originally authored to use conventional vertex
processing, and providing for API features that reduce the effort required to augment an existing
3D application to use application-programmable vertex processing.

11.   It would have been obvious to one of ordinary skill in the art at the time the invention
was made to combine using said second microprocessor to apply a second effect to said first-
effected frame, applying said first effect to a next frame by said first microprocessor
approximately during the time that said second microprocessor is applying said second effect to

said first-effected frame as shown in Glanville with Giles for the benefit of providing a set of

API features that facilitate combining application-programmable vertex processing with existing

3D applications originally authored to use conventional vertex processing, and providing for API

features that reduce the effort required to augment an existing 3D application to use application-

programmable vertex processing.

12.   Regarding claim 77, Giles teaches: The method wherein the first microprocessor is a

CPU and the second microprocessor is a GPU (fig. 4, 140 and 158 see also col. 6 lines 5-11; col.

6 lines 63-67).

13.   Regarding claim 78, Giles teaches: The method where emulation is effected through a

virtual machine (col. 2 lines 20-26).

14.   Regarding claim 79, Giles doesn't teach: The method wherein emulation is effected

through translating a GPU program to a CPU program.

15.   The analogous prior art Glanville teaches: The method wherein emulation is effected

through translating a GPU program to a CPU program [0015] for the benefit of providing a set of

API features that facilitate combining application-programmable vertex processing with existing

3D applications originally authored to use conventional vertex processing, and providing for API

features that reduce the effort required to augment an existing 3D application to use application-

programmable vertex processing.

16.   It would have been obvious to one of ordinary skill in the art at the time the invention

was made to combine emulation is effected through translating a GPU program to a CPU

program as shown in Glanville with Giles for the benefit of providing a set of API features that

facilitate combining application-programmable vertex processing with existing 3D applications

originally authored to use conventional vertex processing, and providing for API features that

reduce the effort required to augment an existing 3D application to use application-

programmable vertex processing.

17.   Regarding claim 80, Giles teaches: A computer-readable medium having computer

executable instructions for performing the method (fig. 4, 144).

Conclusion

18.   **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time

policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE

MONTHS from the mailing date of this action. In the event a first reply is filed within TWO

MONTHS of the mailing date of this final action and the advisory action is not mailed until after

the end of the THREE-MONTH shortened statutory period, then the shortened statutory period

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the mailing

date of this final action.

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to MAURICE MCDOWELL, JR whose telephone number is

(571)270-3707. The examiner can normally be reached on Mon-Friday 7:30am - 5:00pm

Eastern Time.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Xiao Wu can be reached on 571--272-7761. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

MM

/XIAO M. WU/

Supervisory Patent Examiner, Art Unit 2628